IN THE ABSTRACT:

Please replace the Abstract of the Disclosure originally filed with the above-identified patent application with the following new Abstract of the Disclosure:

ABSTRACT OF THE DISCLOSURE

An image processing device includes a high-speed bus and a peripheral bus linked via a bus bridge, and connected to the buses are a CPU for carrying out computations and control of image processing, a data transceiving FIFO memory for carrying out transceiving of image compression data with a host device, a frame memory for storing image expansion data from an electronic camera and the like and displaying the data on a display panel, and a compression/expansion circuit for carrying out compression of image expansion data and expansion of image compression data. The CPU and the frame memory are connected to the high-speed bus and the data transceiving FIFO memory is connected to the peripheral bus. The arrangement of the image processing device makes the CPU operate more efficiently to achieve overall increased speed in image processing.